SETSCI Conference Indexing System, Volume 2 (2018), 376-379

ISAS 2018

1st International Symposium on Innovative Approaches in Scientific Studies

April 11-13, 2018, Kemer-Antalya, Turkey

A Novel Cascade 11 Level Inverter Design

Mehmet Ali Aygül [1*], Nurettin Abut [1] and Umut Özkaya[2]

[1] Department of Electrical Engineering, Kocaeli University, Turkey

[2] Department of Electrical and Electronics Engineering, Selçuk University, Turkey

*Corresponding author: mehmetaliaygul@gmail.com

+Speaker: uozkaya@selcuk.edu.tr

Presentation/Paper Type: Oral / Full Paper

Abstract – Recently, works on the development of equipment in the field of power electronics has been increasing day by day. Inverter design is one of the outstanding issues in the field of power electronics. One of the most important of these studies has been the multi-level inverter topology. Because of their working ability in high power and high efficiency in alternative energy sources, multi-level inverters are preferred. Multilevel inverters have the advantages of lower harmonic on output voltage, lower switching frequency and higher efficiency than conventional inverter designs. In this study, 11 level inverter design is given. The parts forming the inverter structure, the switching method and working principle are explained. The method used to calculate the switching angle and the resulting formulas are presented. Experimental studies were carried out in the Matlab 2017b simulation of multilevel inverter. The designed inverter produces low harmonic output voltage and reduces the dv / dt stress stress on the switching elements. The obtained results can be used in real time applications.

Keywords – Power Electronics, Multi-level Inverter, Level Module, H Bridge, Inverter Design

I. Introduction

Inverters has become an indispensable element for many industrial applications today. In control of various engine types and power systems, inverters are widely used. There are also more usage of inverters in systems where battery systems, fuel cells, solar batteries, wind turbines or micro turbines feed a load or network. Due to this reason, studies on inverters are increasing and accordingly inverter technology is rapidly developing. The main aim in all the studies is to obtain the output voltage and load current with better quality by keeping the number of switches at the minimum level. As a result of the studies made for this purpose, many new structures have been obtained and new switching techniques have been developed on these structures. In multi-level inverters, as the number of levels increases, the change in output voltage is more similar to the sinus signal [1]. For this reason, works in multilevel inverters design has been increased to achieve high quality current and voltage signals.

In recent years, high power and low harmonic demand in alternating current power supplies has been increasing steadily. In the case where these sources feed a load or network, it is desirable that the voltage waveform of the inverter output voltage is very sinusoidal because the harmonic levels are too low. [2,3] This can also be achieved using multi-level inverter topologies. Multi-level inverter topologies in the literature can be basically classified into three groups called diode-clamped, flying-capacitor and cascaded inverters. There are also cascaded transformers and cascaded half H-bridge inverters in the literature.

Since multilevel inverters have gradual voltage levels, the dv / dt voltage stress on the switching elements is low and the output voltage is high. Low efficiency and electromagnetic interference problems arise due to the high switching frequency of the pulse width ratio (PWR) inverter and the high dv / dt stress of these inverters. As a result, the output filter must be used to reduce high switching frequency components and to obtain sinusoidal output voltage in series. To avoid these problems, multi-level inverters compete with classic PWR inverters [4] - [6].

Depending on the developments in inverter technology, a novel multilevel inverter structure and the switching method to be used in this structure have been developed. The parts constituting the inverter structure are introduced, and the operation principle of inverter is given. Procedures for increasing the number of voltage levels have been described. With the developed method, the switching functions are obtained according to the switching directions. Section 2 includes details of elements in cascade 11-level inverter design and working principles. The experimental results of the design performed in Section 3 are interpreted. Section 4 is final section which contains conclusions and discussion.

II. Materials and Method

The principle diagram of the multi-level inverter prototype shown in Fig. 1. The designed 11-level inverter is basically composed of two modules. These are level modules and H-bridge module. A phase inverter used in design has a very suitable structure to expand. By increasing the number of level modules in the structure, the number of levels of output voltage can be easily increased.

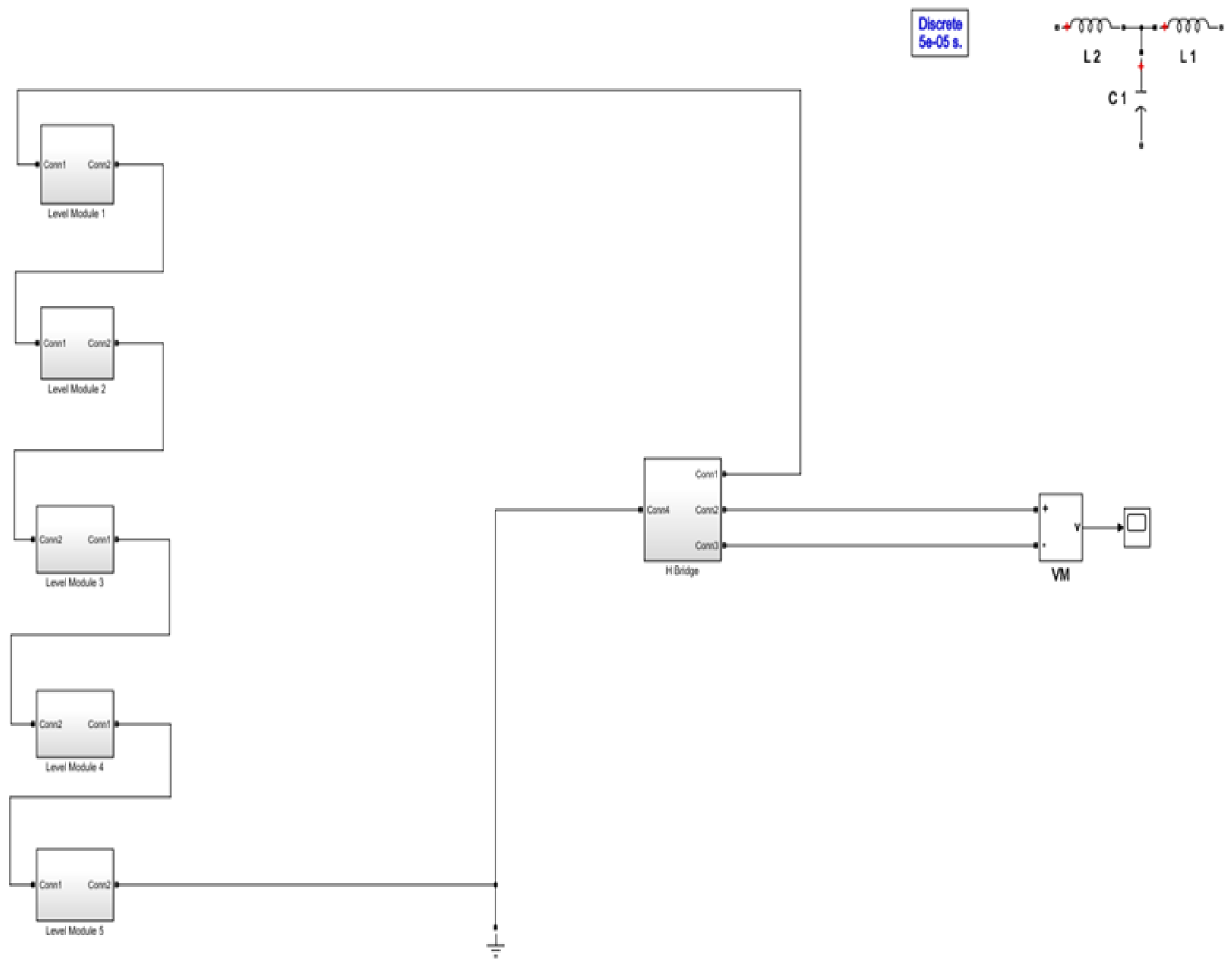

Fig. 1. Inverter Structure

A. Level Module

The level module consists of 1 switching element and 1 direct current source. The voltage of the source in each level module,

$$2^{(k-1)}.V_d \tag{1}$$

In this equation, $k = 1,2,3 \ldots m$. Also, m is the number of level modules found in one-phase inverters and V_d is the voltage of the first level [7].

$$V_d = \frac{2.V_{max}}{n_{fn}-1} \tag{2}$$

Where V_{max} is the maximum value of the voltage change in one phase and n_{fn} is the number of levels of the phase-neutral voltage [8]. Fig. 2 shows the principle diagram of the level module.

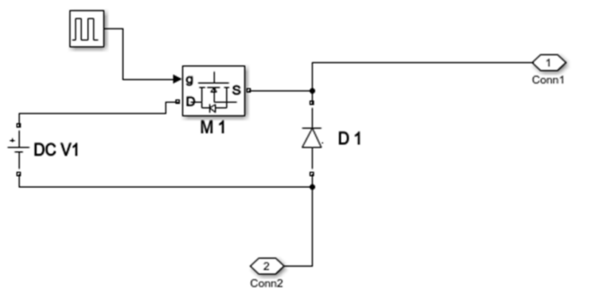

Fig. 2. Level Module Implementation

B. H Bridge

The structure of the H-Bridge module is the same as that of the conventional H-Bridge inverter. The H-bridge module is the fixed part in the inverter system and as can be understood from Figure 1, there is an H-bridge module in each phase. The principle diagram of the H-bridge module is shown in Fig. 3.

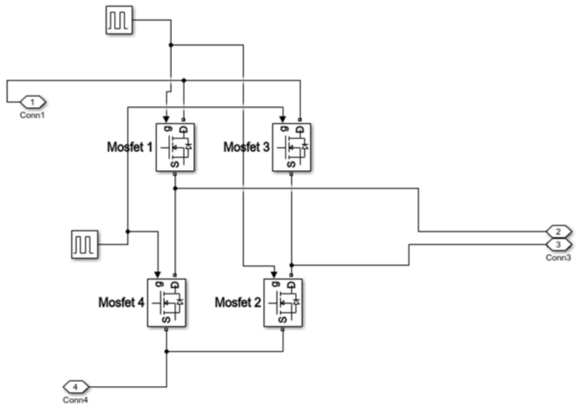

Fig. 3. H Bridge

The multilevel inverter structure in this work will be called binary cascade because the source voltage values change in multiples of two as in the binary number system. Thanks to this structure, the number of auxiliary switching elements and the resources can be increased to easily increase the number of levels. Compared with classical multilevel inverters, the increase in the number of switching elements is less as the number of levels increases.

There is a correlation between the number of level modules and the number of switching elements and the number of levels of output voltage. These relations are given in Eqs. (3) and (4) [9].

$$\mathrm{n}_{fn} = 2^{(m+1)} - 1 \tag{3}$$

$$\mathrm{r}_{1\varphi} = 2m + 4 \tag{3}$$

n_{fn} is the number of levels of phase-neutral voltage. $r_{1\varphi}$ represents the number of switching elements of the 1-phase inverter [10].

III. Results

Eleven level inverter designs have been realized for the same switching frequency, modulation index, output frequency and load values. The switching frequency was chosen to be 20 kHz, L = 0.01 H and C = 2.10^{-6} F. The voltage graph of the eleven level inverter is given in Figure 4.

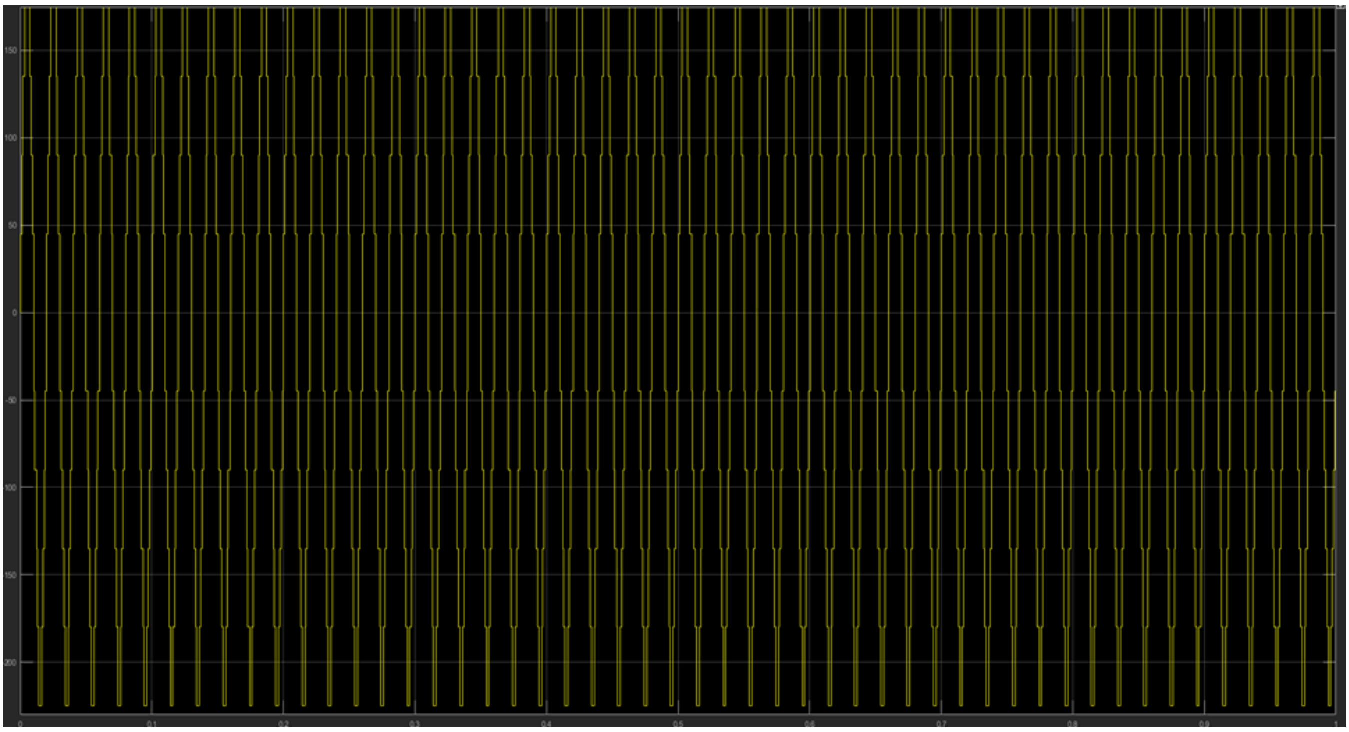

Fig. 4. Simulation Result

The designed multi-level inverter prototypes were firstly simulated. Then a series of experimental studies were carried out by producing an inverter. Simulation and experimental results of multi-level inverter are given in Figure 4.

IV. Conclusion and Discussion

In this study, a new structure was developed by developing the methods available in the literature. The method used for calculation of the switching angles and the formula obtained as a result are presented. Accordingly, the switching angles can easily be calculated by the proposed method. The designed inverter has a very suitable structure to expand. With the added resources, the number of levels increases exponentially. As the number of levels increases, the total harmonic distortion decreases and it is seen in the experimental results. The designed inverter significantly reduces the dv / dt stress on the switching elements and produces good output voltage.

References

[1] Çamur S., Arifoğlu B., Beşer E. Kandemir and Beşer E., “Design and Application of a Novel Structure and Topology for Single-Phase Five-Level Inverter”, Wseas Transactions on Electronics, 2006.

[2] Hua,C.C., Wu,C.H. and Chuang,C.W., "Control of Low-Distortion 27-Level Cascade Inverter with Three H-Bridge Inverter Modules”, IEEE Power Electronics, pp.277-282, 2006.

[3] Khersonsky, Y., (2003). Step Switched PWM Sine Generator, U.S. patent number 06,556,461, assigned to Power Paragon Incorporated, April 2003.

[4] Fracchia, M., Ghiara, T., Marchesoni, M. Ve Mazzucchelli, M., (1992). "Optimized Modulation Techniques for the Generalized N-Level Converter", Proceedings of the IEEE Power Electronics Specialist Conference, 1992.

[5] Rodriguez, J., Lai, J.S. ve Peng, F.Z., (2002) “Multilevel inverters: A survey of topologies, controls, and applications,” IEEE Trans. Ind. Electron., 49(4):724–738.

[6] Kouro, S., Malinowski, M., Gopakumar, K., Pou, J., Franquelo, L.G., Wu, B., Rodriguez, J., Pérez, M.A. ve Leon, J.I., (2010). “Recent Advances and Industrial Applications of Multilevel Converters”, IEEE Transactions on Industrial Electronics, 57(8):2553-2580.

[7] Haiwen, L., Tolbert, L. M., Khomfoi, S., Ozpineci, B. ve Zhong, D., Hybrid Cascaded Multilevel Inverter with PWM Control Method, 39th Annual Power Electronics Specialists Conference (PESC’08), June 2008, Greece, 162–166.

[8] Khoukha, I., Hachemi, C. ve El Madjid, B., Multilevel Selective Harmonic Elimination PWM Technique in the Nine Level Voltage Inverter, International Conference on Computer Engineering and Systems (ICCES), November 2007, Cairo, Egypt, 387-392.

[9] Ebrahimi, A., Farokhnia, N. ve Fathi, S. H., A Hybrid Approach for Solving Nonlinear Equations of SHEPWM in Multilevel Inverters, IEEE International Symposium on Industrial Electronics, (2012) 1962–1967.

[10] Pulikanti, S. R., Konstantinou, G. ve Agelidis, V. G., Hybrid Seven-Level Cascaded Active Neutral-Point-Clamped-Based Multilevel Converter Under SHE-PWM. IEEE Transactions Industrial Electronics, 60, 11 (2013) 4794-4804.